REMARKS

Claims 1-7, 15-26, and 30-32 are pending. Claims 1, 15, and 19 are in independent form.

CLAIM 1

In the action mailed November 17, 2005, claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,933,627 to Parady (hereinafter "Parady") and pages 173-176 and 200 of the publication entitled "Computer Systems Design and Architecture" by Heuring and Jordan (hereinafter "Heuring").

Claim 1 relates to an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the arithmetic logic unit. The register set comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Each bank is capable of performing a read and a write to two different words in the same processor cycle.

The rejection of claim 1 contends that both Parady and Heuring describe a register set that comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Applicant respectfully disagrees.

Applicant submits that Parady and Heuring both describe standard, multi-ported devices rather than a register set that comprises a plurality of two-ported random access memory devices. In regard to Parady, the rejection contends that Parady's integer registers 48 constitute a register set that comprises a plurality of two-ported random access memory devices. However, Paraday is silent as to the architecture of integer registers 48. Indeed, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1. Certainly nothing about Parady's registers describes or suggests that integer registers 48 comprise a plurality of two-ported random access memory devices.

Indeed, the only mention of two-ported register files made in Parady is found at col. 5, line 30-43. In this section, Parady acknowledges that multi-ported register files can occupy more silicon that simple duplication of registers. However, the duplication of dual ported register files described by Parady does not suggest a register set that comprises a plurality of two-ported random access memory devices and that includes two

effective read ports and one effective write port. For example, FIG. 7 illustrates how Parady envisages dual ported register files can be duplicated. In particular, dual ported shadow registers 186 are to be individually addressed using a data switch 192 or individually enabled for writing along a path 194. Such individual addressing or individual enablement does not provide a register set that comprises two-ported random access memory devices and includes two effective read ports and one effective write port, as recited in claim 1. Rather, individual addressing or individual enablement of a dual ported register file inherently limits the effective ports to two—i.e., the two ports on the individually addressed or individually enabled dual ported register file.

Heuring adds nothing to remedy this deficiency in Parady. Heuring describes a well-known multi-ported processor that includes a 3-ported register file. Every element in Huering's register file has three ports and every element suffers from the silicon consumption disparaged by Parady. This is further evidenced by the small size of Huering's device, which includes only 32 registers.

There is no description or suggestion in Heuring that this 3-ported register file comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Rather, the 3-ported

register file appears to be a standard multi-ported register file.

Since elements and/or limitations of claim 1 are neither described nor suggested by the cited art, a *prima facie* case of obviousness has not been established. Accordingly, Applicant requests that claim 1, and the claims dependent therefrom, be allowed.

CLAIM 15

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Heuring.

Claim 15 relates to a method for executing multiple context threads. The method includes processing data for executing threads within an arithmetic logic unit, operating control logic to control the arithmetic logic unit, and storing and obtaining operands for the arithmetic logic unit within a general purpose register set. The general purpose register set comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Each bank is capable of performing a read and a write to two different words in the same processor cycle.

The rejection of claim 15 points to the rejection of claim 1 and contends that both Parady and Heuring describe storing and obtaining operands within a general purpose register set that comprises a plurality of two-ported random access memory devices

and includes two effective read ports and one effective write port. Applicant respectfully disagrees.

As discussed above, Parady and Heuring both describe standard, multi-ported devices rather than a register set that comprises a plurality of two-ported random access memory devices. Paraday is silent as to the architecture of integer registers 48. Moreover, Parady's duplicated dual ported register files are to be individually addressed using or individually enabled, which inherently limits the effective ports to two.

Heuring adds nothing to remedy this deficiency in Parady. There is no description or suggestion in Heuring that the 3-ported register file comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Rather, the 3-ported register file appears to be a standard multi-ported register file.

Since elements and/or limitations of claim 15 are neither described nor suggested by the cited art, a *prima facie* case of obviousness has not been established. Accordingly, Applicant requests that claim 15, and the claims dependent therefrom, be allowed.

CLAIM 19

Claim 19 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Heuring.

Claim 19 relates to a processor unit that includes an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the arithmetic logic unit. The register set comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port.

The rejection of claim 19 contends that both Parady and Heuring describe a register set that comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Applicant respectfully disagrees.

As discussed above, Parady and Heuring both describe standard, multi-ported devices rather than a register set that comprises a plurality of two-ported random access memory devices. Parady is silent as to the architecture of integer registers 48. Moreover, Parady's duplicated dual ported register files are to be individually addressed using or individually enabled, which inherently limits the effective ports to two.

Heuring adds nothing to remedy this deficiency in Parady. There is no description or suggestion in Heuring that the 3-ported register file comprises a plurality of two-ported random access memory devices and includes two effective read ports and one effective write port. Rather, the 3-ported register file appears to be a standard multi-ported register file.

Since elements and/or limitations of claim 19 are neither described nor suggested by the cited art, a *prima facie* case of obviousness has not been established. Accordingly, Applicant requests that claim 19, and the claims dependent therefrom, be allowed.

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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